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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,306	03/14/2001	Kenichi Kawaguchi	NAK1-BG45a	2445

7590 03/25/2004

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EXAMINER

SHRADER, LAWRENCE J

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/808,306

Applicant(s)

KAWAGUCHI, KENICHI

Examiner

Lawrence Shrader

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/04/2001; and 3/14/2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21 - 23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21 - 23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/280,363.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. This action is in response to the preliminary amendment filed on 3/14/2001 as a divisional application of 09/280,363 now U.S. Patent 6,360,312.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 3/14/2001 is acknowledged. Accordingly, the information disclosure statement has been considered by the examiner.

Drawings

3. The drawings received on 6/04/2001 are acknowledged.

Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 21 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto et al., U.S. Patent 6, 496, 919 (hereinafter referred to as Nishimoto) in view of Tanaka et al.,

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U.S. Patent 5,923,883 (hereinafter referred to as Tanaka), and further in view of Nakahara, U.S. Patent 5,701,425.

In regard to claim 21:

A program conversion apparatus that changes a source program to an object program for a target processor executing long-word instructions, comprising:

a retrieving unit, for retrieving a pair of instructions from the source program, the pair of instructions comprising a first instruction denoting a first calculation of two variables and a second instruction indicating a second calculation, different than the first calculation, of the same two variables;

Nishimoto discloses a compiler integrated in a very long-word instruction (VLWI) system to combine executable instructions to improve operating speed (column 1, line 50 – column 2, line 11), but does not explicitly disclose retrieval of an instruction sequence from a source program, receiving a pair of instructions, the first denoting a first calculation of two variables, and a second instruction of the same two variables. However, Tanaka teaches a pair of instructions, the first denoting a first calculation (add) of two variables (r1 and r2), and a second instruction (subtract) of the same two variables r1 and r2 (e.g., see Figure 1). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the combining of the very-long instruction word instructions of Nishimoto with the retrieval of pairs of instructions operating on the same variables, because the modification gives the system of Nishimoto higher speed performance by checking dependencies and simultaneously executing two instructions as one instruction as taught by Nishimoto at column 2, lines 1 – 10.

a generating unit, for generating a special instruction corresponding to the retrieval pair of instructions, the special instruction comprising an operation code denoting the first calculation and the second calculation, and two operands representing the two variables; and

an arranging unit, for arranging the generated special instruction into a long-word instruction.

Nishimoto discloses a compiler integrated in a very long-word instruction (VLWI) system to combine executable instructions to improve operating speed (column 1, line 50 – column 2, line 11), but neither Nishimoto nor Tanaka discloses a process of combining op-codes to create a special instruction operating on the same two variables. However, Nakahara discloses data processor that combines op-codes and operands (column 13, lines 40 – 44). Therefore, it would have been obvious one skilled in the art at the time the invention was made to modify the teaching of Nishimoto compiling code by combining the very-long instruction word instructions into one instruction with the teaching of Tanaka which retrieves of a pair of instructions operating on the same operands, and further modified the with the combining of op-codes as taught by of Nakahara, because the modifications produce a combination that allows the apparatus to compile code by combining op-codes and the associated operands into a compact function generating a special instruction, which diversifies the processing ability without increasing number of instructions in the instruction set of the code as taught by Nakahara at column 13, lines 18 – 27.

In regard to claim 22, incorporating the rejection of claim 21:

"...wherein the first instruction denotes addition, and the second instruction denotes subtraction."

Nishimoto discloses an integer arithmetic set (column 10, lines 63 – 65), however Tanaka discloses retrieval of an instruction sequence from a source program, receiving a pair of instructions, the first denoting a first calculation (add) of two variables r1 and r2, and a second

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instruction (subtract) of the same two variables r1 and r2 (e.g., see Figure 1). Therefore it would have been obvious to one skilled in the art at the time the invention was made to combine the arithmetic unit as taught by Nishimoto with the instruction sequence of Tanaka, which provides an arithmetic execution of the sequence of instructions disclosed in Tanaka.

In regard to claim 23, incorporating the rejection of claim 22:

"...wherein the target processor includes a first instruction execution unit having a first calculation unit, and a second instruction execution unit having a second calculation unit and a multiplication unit; and"

Nishimoto discloses a first execution unit having a calculation unit, and a second instruction execution unit having a second calculation unit and a multiplication unit (e.g., Figure 7; column 10, line 54 to column 11, line 23)

the arranging unit retrieves a multiply instruction that does not share dependency with the special instruction generated by the generating unit, and arranges the special instruction and the multiply instruction into one long-word instruction.

See Nishimoto Figure 7, ref 131 and related text at column 11, lines 5 – 23.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 6,151,618 to Wahabe et al., regarding op-code combining techniques.

U.S. Patent 6,675,376 to Ronen et al., regarding combining instructions to create a new instruction having an op-code representing the operation performed by the first and second instructions, and having operands representing the operands of the first and second instructions.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046.

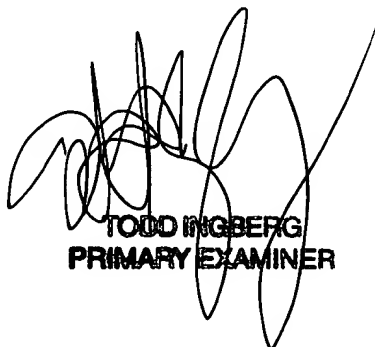
The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence Shrader
Examiner
Art Unit 2124

19 March 2003



TODD INGBERG
PRIMARY EXAMINER